REMARKS

Applicants have studied the Office Action dated November 14, 2002 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1-23 and 30-34 are pending. Claims 27-29 have been canceled without prejudice. Claims 1, 7, 8, 14, 15, 19, and 20 have been amended, and new claims 30-34 have been added. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

As an initial matter, Applicants note that while a certified copy of the document from which the present application claims priority was submitted on December 18, 2001, the Examiner did not properly indicate that "All certified copies of the priority documents have been received" (i.e., box 13(a)(1) was not checked). Because the certified copy of the document from which the present application claims priority has been submitted, it is requested that the Examiner clarify the situation by properly indicating in the next correspondence that all of the certified copies of the priority documents have been received.

Turning to the patentability of the application, claims 3 and 10 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification. The Examiner stated that the specification does not recite any description of the steps for incorporating an inductor into the circuit. This rejection is respectfully traversed.

Claims 3 and 10 recite an integrated circuit that includes a passive component in the form of an inductor. The specification states in several places that the passive component can be a capacitor or an inductor. See specification at 8:13-14; 13:12-16; 14:26-29. Furthermore, while the present invention is described in detail in the specification with reference to an exemplary embodiment in which the passive component is a capacitor, the specification goes on to state that the present invention can be applied in the same way to other types of passive components such as resistors and inductors. As an example of such an embodiment, the specification states that "it

is possible to substitute a copper inductor formed by a damascene process (using a similar cavity) for the capacitor formed in the exemplary fabrication process shown in the figures." See specification at 14:19-25.

Applicants submit that one of ordinary skill in the art of integrated circuit fabrication would know how to form an inductor in place of the capacitor of the exemplary embodiment, such as by using a damascene process to form a copper inductor as suggested in the specification. See, e.g., U.S. Patent Nos. 5,793,272, 6,187,647, and 6,291,872. Thus, Applicants respectfully submit that the description in the specification enables one of ordinary skill in the art to make and/or use an integrated circuit that includes a passive component in the form of an inductor. Accordingly, it is respectfully submitted that the rejection of claims 3 and 10 under 35 U.S.C. § 112, first paragraph, should be withdrawn.

Claims 27-29 were also rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification. Claims 27-29 have been canceled so this rejection is moot.

Claims 1, 2, 4-9, and 11-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Okumura (U.S. Patent No. 6,333,535) in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publications, pp. 157, 868). This rejection is respectfully traversed.

The present invention is directed to providing a low-resistance electrical contact between a passive component and another component of an integrated circuit. One embodiment provides an integrated circuit having a plurality of active components and at least one passive component situated above the active components. The integrated circuit includes a first insulating layer that separates the active components and a base of the passive component, and a metal terminal that electrically connects the passive component with at least one of the active components. The metal terminal is formed in the thickness of the first insulating layer and has a lower surface that contacts a junction of the one active component such that the lower surface of the metal terminal

extends over a boundary of the junction of the one active component. Because the lower surface of the metal terminal extends over the boundary of the junction of the active component, the contact resistance is reduced and dopant atoms are prevented from penetrating as far as the junction of the active component.

The Okumura reference discloses a semiconductor device in which wiring layers and semiconductor layers are electrically connected through buried polysilicon layers. However, Okumura does not disclose an integrated circuit having active components and at least one passive component that includes a first insulating layer separating the active components and a base of the passive component, and a metal terminal formed in the thickness of the first insulating layer and having a lower surface that contacts a junction of one of the active components such that the lower surface extends over a boundary of the junction of the active component, as is recited in amended claim 1.

Likewise, Okumura does not disclose an integrated circuit including transistors, passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors, with the integrated circuit including a second metal terminal that vertically connects an active area of the integrated circuit to a passive component that directly contacts the upper surface of the first insulating layer, as is recited in amended claim 7. Amended claims 14 and 19 contain similar recitations.

The semiconductor device disclosed in Okumura has cylindrical capacitors and transistors as active components. As shown in Figures 10A and 10B, some connectors 32 pass through three insulating layers 11, 17, and 23 to electrically connect the active components to an overlying wiring layer 25. Other connectors 13 pass through the first insulating layer 11 to electrically connect the active components to horizontal connections 16 that are provided on the first insulating layer 11. Additionally, a junction 71 of one of the active components is connected to one plate 19 of a capacitor by a connector 31 that passes through the first and second insulating layers 11 and 17.

In the semiconductor device of Okumura, the connector 31 for electrically connecting to the capacitor has a lower surface that contacts only an interior portion of the junction 71 of the active component. Thus, the lower surface of this connector does not extend over any boundary

of the junction of the active component. Further, in the semiconductor device of Okumura, the capacitor is formed above both the first and second insulating layers 11 and 17. Thus, the capacitor does directly contact the upper surface of the insulating layer that is deposited on top of the transistors of the integrated circuit (i.e., the first insulating layer).

In contrast, in the embodiment of the present invention recited in amended claim 1, the metal terminal for electrically connecting to the passive component (e.g., capacitor) has a lower surface that extends over the boundary of the junction of the active component. For example, in the exemplary embodiment shown in Figures 5 and 6, a metal terminal 107 provides a vertical connection between one of the two junctions 104 of a transistor T in an active area 109 and the bottom electrode 126 of a capacitor C. The terminal 107 projects from (i.e., extends over the boundary of) the junction 104 (i.e., the doped monocrystalline silicon of region). In other words, the terminal 107 extends right through and straddles the boundary between the junction 104 and the adjacent dielectric material trench 101. This advantageously reduces the contact resistance and prevents dopant atoms from penetrating as far as the junction of the active component. Okumura does not teach or suggest an integrated circuit in which a metal terminal for electrically connecting to a passive component has a lower surface that extends over the boundary of the junction of an active component.

Additionally, in the embodiments of the present invention recited in amended claims 7, 14, and 19, the passive component (e.g., capacitor) directly contacts the upper surface of the insulating layer that is deposited on top of the transistors of the integrated circuit. For example, in the exemplary embodiment shown in Figures 5 and 6, a first insulating layer 105 is deposited over the transistors T formed in the substrate 100. A second insulating layer 113 is then deposited on the first insulating layer 105. A cavity 116 is etched in the second insulating layer 113 such that the cavity 116 penetrates to the upper surface of the first insulating layer 105. A capacitor C is then formed inside the cavity 116 such that the bottom electrode 126 of the capacitor C directly contacts the upper surface of the first insulating layer 105. A metal terminal 107 provides a vertical connection between an active area 109 and the bottom electrode 126 of the capacitor C. Okumura does not teach or suggest an integrated circuit having a metal terminal

that vertically connects an active area to a passive component that directly contacts the upper surface of the insulating layer that is deposited on top of the transistors of the integrated circuit.

Furthermore, the claimed features of the present invention are not realized even if the teachings of Wilson are incorporated into Okumura.[1] Wilson does not teach or suggest the claimed features of the present invention that are absent from Okumura. Applicants believe that the differences between Okumura, Wilson, and the present invention are clear in amended claims 1, 7, 14, and 19, which set forth various embodiments of the present invention. Therefore, claims 1, 7, 14, and 19 distinguish over the Okumura and Wilson references, and the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

As discussed above, claims 1, 7, 14, and 19 distinguish over the Okumura and Wilson references, and thus, claims 2 and 4-6, claims 8, 9, and 11-13, claims 15-18, and claims 20-23 (which depend from claims 1, 7, 14, and 19, respectively) also distinguish over the Okumura and Wilson references. Therefore, it is respectfully submitted that the rejection of claims 1, 2, 4-9, and 11-23 under 35 U.S.C. § 103(a) should be withdrawn.

Claims 30-34 have been added by this amendment, and are provided to further define the invention disclosed in the specification. Claims 30-34 are allowable for at least the reasons set forth above with respect to claims 1-23.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

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[1] Applicants make no statement as to whether such a combination is even proper.

Respectfully submitted,

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By: ______________________

Stephen Bongini
Registration No. 40,917
Attorney for Applicants

FLEIT, KAIN, GIBBONS,
GUTMAN & BONGINI P.L.
One Boca Commerce Center
551 Northwest 77th Street, Suite 111
Boca Raton, Florida 33487
Telephone: (561) 989-9811
Facsimile: (561) 989-9812

APPENDIX

IN THE CLAIMS:

1. (Amended) An integrated circuit having a plurality of active components including junctions formed in a monocrystalline substrate doped locally, and at least one passive component situated above the active components, said integrated circuit comprising:

a first insulating layer separating the active components and a base of the passive component; and

a metal terminal for electrically connecting the passive component with at least one of the active components, the metal terminal being formed in the thickness of the first insulating layer and having a [contact] lower surface that [projects from the limits of a] contacts a junction of the one active component such that the lower surface of the metal terminal extends over a boundary of the junction of the one active component.

7. (Amended) An integrated circuit including a plurality of transistors, a plurality of passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors of the integrated circuit, said integrated circuit comprising:

a first metal terminal passing completely through the thickness of the first insulating layer, the first metal terminal constituting a first stage of contact between an active area of the integrated circuit and a first level of interconnection;

a second metal terminal passing completely through the thickness of the first insulating layer, the second metal terminal vertically connecting an active area of the integrated circuit to a passive component that directly contacts the upper surface of [resting on] the first insulating layer; and

a third metal terminal passing completely through the thickness of the first insulating layer, the third metal terminal horizontally connecting two separate active areas of the integrated circuit.

8. (Amended) The integrated circuit according to claim 7, wherein the second metal terminal has a [contact] <u>lower</u> surface [projecting from the limits of a] <u>that contacts a junction of one of the transistors of the integrated circuit such that the lower surface of the metal terminal extends over a boundary of the</u> junction of [an active component] <u>the one transistor</u>.

14. (Amended) An integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, <u>the one plate of the one storage capacitor directly contacting the upper surface of the first insulating layer,</u> and

the third metal terminal horizontally connects two separate active areas of the integrated circuit.

15. (Amended) The integrated circuit according to claim 14, wherein the second metal terminal has a [contact] <u>lower</u> surface [projecting from the limits of a] <u>that contacts a junction of the one active area such that the lower surface of the metal terminal extends over a boundary of the</u> junction of the <u>one</u> active area.

19. (Amended) An information processing system including at least one integrated circuit, the integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, the one plate of the one storage capacitor directly contacting the upper surface of the first insulating layer, and

the third metal terminal horizontally connects two separate active areas of the integrated circuit.

20. (Amended) The information processing system according to claim 19, wherein the second metal terminal has a [contact] lower surface [projecting from the limits of a] that contacts a junction of the one active area such that the lower surface of the metal terminal extends over a boundary of the junction of the one active area.